This listing of claims will replace all prior versions of claims in the Application.

Listing of Claims

Claim 1. (Currently Amended) A method for electroplating a plurality of electronic devices, each electronic device having apertures and comprising a copper containing seed layer ~~comprising~~, wherein a layer of metal electroplated on the seed layer of a first electronic device to at least substantially fill the apertures has voids, comprising the steps of:

a) ~~electroplating a layer of metal on the seed layer of a first electronic device to at least substantially fill the apertures;~~

~~b) testing the first electronic device for voids in the apertures;~~

~~c) if no voids exist in step b), electroplating a layer of metal on the seed layer of the remaining electronic devices;~~

~~d) if voids exist in step b),~~ subjecting a second electronic device to a seed layer repair process selected from cathodic activation or lateral growth enhancement, followed by electroplating a layer of metal on the seed layer of the second electronic device to at least substantially fill the apertures;

~~e~~b) testing the second electronic device for voids in the apertures;

~~f~~c) if no voids exist in step ~~e~~b), electroplating a metal layer on the seed layer of the remaining electronic devices to at least substantially fill the apertures following the process of step ~~d~~a);

~~g~~d) if voids exist in step ~~e~~b), subjecting a third electronic device to a seed layer repair process selected from cathodic activation or lateral growth enhancement, followed by electroplating a layer of metal on the seed layer of the third electronic device to at least substantially fill the apertures, provided that the seed layer repair process is different from the seed layer repair process of step ~~d~~a);

~~h~~e) testing the third electronic device for voids in the apertures;

~~i~~f) if no voids exist in step ~~h~~e), electroplating a metal layer on the seed layer of the remaining electronic devices to at least substantially fill the apertures following the process of

step gd);

jg) if voids exist in step he), subjecting the remaining electronic devices to a seed layer repair process selected from cathodic activation plus lateral growth enhancement or cathodic activation plus solution seed layer deposition, followed by electroplating a metal layer on the seed layer of the remaining electronic devices to at least substantially fill the apertures.

Claim 2. (Original) The method of claim 1 wherein the seed layer is a copper alloy.

Claim 3. (Original) The method of claim 1 wherein the plurality of electronic devices is a plurality of wafers.

Claim 4. (Original) The method of claim 1 wherein each of the electronic devices further comprises a barrier layer.

Claim 5. (Currently Amended) The method of claim 4 wherein the barrier layer is selected from tantalum, tantalum nitride, titanium, titanium nitride, tungsten, tungsten nitride, molybdenum, molybdenum nitride, cobalt, and cobalt nitride.

Claim 6. (Original) The method of claim 1 wherein the apertures have a width ≤ 1 μm.

Claim 7. (Original) The method of claim 1 wherein the apertures have an aspect ratio of from 1:1 to 10:1.

Claim 8. (Currently Amended) A method for ~~electroplating~~ manufacturing a plurality of electronic devices, each electronic device having apertures and comprising a copper containing seed layer, wherein a layer of metal electroplated on the seed layer of a first electronic device to at least substantially fill the apertures has voids, the seed layer of the first electronic device being subjected to a step of cathodic activation, comprising the steps of:

a) ~~subjecting a first electronic device to a cathodic activation step;~~

~~b) electroplating a layer of metal on the seed layer of the first electronic device to at least substantially fill the apertures;~~

~~c) testing the first electronic device for voids in the apertures;~~

~~d) if no voids exist in step c), subjecting the remaining electronic devices to a cathodic activation step followed by electroplating a layer of metal on the seed layer of the remaining~~

~~electronic devices;~~

~~c) if voids exist in step c),~~ subjecting the remaining ~~wafers~~ electronic devices to a cathodic activation step plus a seed layer repair process selected from lateral growth enhancement ~~or~~ and solution seed layer deposition, followed by electroplating a layer of metal on the seed layer of the remaining electronic devices to at least substantially fill the apertures.

Claim 9. (Original) The method of claim 8 wherein the plurality of electronic devices is a plurality of wafers.

Claim 10. (Original) The method of claim 8 wherein each of the electronic devices further comprises a barrier layer.

Claim 11. (Currently Amended) The method of claim 10 wherein the barrier layer is selected from tantalum, tantalum nitride, titanium, titanium nitride, tungsten, tungsten nitride, molybdenum, molybdenum nitride, cobalt, and cobalt nitride.

Claim 12. (Currently Amended) ~~the~~ The method of claim 8 wherein the apertures have a width ≤ 1 μm.

Claim 13. (Original) The method of claim 8 wherein the apertures have an aspect ratio of from 1:1 to 10:1.

Claim 14. (Currently Amended) A method for manufacturing a plurality of electronic devices, each electronic device having apertures and comprising a copper containing seed layer, wherein a layer of metal electroplated on the seed layer of a first electronic device to at least substantially fill the apertures has voids, comprising the steps of:

a) ~~electroplating a layer of metal on the seed layer of a first electronic device to at least substantially fill the apertures;~~

~~b) testing the first electronic device for voids in the apertures;~~

~~c) if no voids exist in step b), electroplating a layer of metal on the seed layer of the remaining electronic devices;~~

~~d) if voids exist in step b),~~ subjecting a second electronic device to a seed layer repair process selected from cathodic activation ~~or~~ and lateral growth enhancement, followed by

electroplating a layer of metal on the seed layer of the second electronic device to at least substantially fill the apertures;

e<u>b</u>) testing the second electronic device for voids in the apertures;

f<u>c</u>) if no voids exist in step e<u>b</u>), electroplating a metal layer on the seed layer of the remaining electronic devices following the process of step d<u>a</u>);

g<u>d</u>) if voids exist in step e<u>b</u>), subjecting a third electronic device to a seed layer repair process selected from cathodic activation or lateral growth enhancement, followed by electroplating a layer of metal on the seed layer of the third electronic device to at least substantially fill the apertures, provided that the seed layer repair process is different from the seed layer repair process of step d<u>a</u>);

h<u>e</u>) testing the third electronic device for voids in the apertures;

i<u>f</u>) if no voids exist in step g<u>d</u>), electroplating a metal layer on the seed layer of the remaining electronic devices <u>to at least substantially fill the apertures</u> following the process of step g<u>d</u>);

j<u>g</u>) if voids exist in step g<u>d</u>), subjecting the remaining electronic devices to a seed layer repair process selected from cathodic activation plus lateral growth enhancement ~~or~~ <u>and</u> cathodic activation plus solution seed layer deposition, followed by electroplating a metal layer on the seed layer of the remaining electronic devices <u>to at least substantially fill the apertures</u>.

Claim 15. (Original) The method of claim 14 wherein the plurality of electronic devices is a plurality of wafers.

Claim 16. (Original) The method of claim 14 wherein each of the electronic devices further comprises a barrier layer.

Claim 17. (Original) The method of claim 14 wherein the apertures have a width ≤ 1 μm.

Claim 18. (Original) The method of claim 14 wherein the apertures have an aspect ratio of from 1:1 to 10:1.

Claim 19. (Canceled)